CLAIMS

1. Volatile Random Access Memory comprising one-transistor cells in which a diode is substituted for the capacitor between the control gate and floating gate and information is read by sensing resistance between the source and drain terminals of the transistor.

2. Dynamic Nonvolatile Random Access Memory comprising one- transistor cells with diode isolation of the transistor gates in which the charging and discharging of the gates through the diode does not change the electrical properties of the material forming the diode and does not stress the gate oxide.

3. Dynamic Nonvolatile RAM as claimed in claim 2 in which the number of writing cycles is sufficiently high and the speed of charging and discharging is sufficiently quick to allow for real time data processing.

4. Dynamic Nonvolatile RAM comprising one-transistor cells in which a silicon carbide device is substituted for the capacitor between the control gate and floating gate and information is read by sensing resistance between the source and drain terminals of the transistor.

5. Dynamic Nonvolatile Random Access Memory as claimed in claim 4 in which the silicon carbide device is a diode.

6. Dynamic Nonvolatile Random Access Memory as claimed in claim 4 in which the silicon carbide device is a controlled switch.

7. Dynamic Nonvolatile Random Access Memory as claimed in claim 4 in which the silicon carbide is a 3C SiC wafer.

8. Dynamic Nonvolatile Random Access Memory as claimed in claim 5 in which the diode is implemented in silicon carbide with the SiC-SiO_2 interface passivated to create charge retention times sufficiently long to avoid the need for the 1T memory cell to be electrically refreshed.

9. Dynamic Nonvolatile Random Access Memory as claimed in claim 7 in which the charge retention times are greater than 7 years.

10. Dynamic Nonvolatile RAM as claimed in claim 8 in which the SiC-SiO_2 interface is nitrided in either NO or N_2O rich environments.

11. NVRAM in which the electron-hole generation/recombination rate and charge leakage are reduced so much that a non-equilibrium charge can be maintained for substantial periods of time, which includes a silicon carbide transistor used as a switch to connect memory cells.

12. A dynamic NVRAM consisting of a one transistor cell wherein the transistor is created with:
    (a) polysilicon body,
    (b) metal or heavily-doped polysilicon contacts acting as source and drain regions, and
    (c) a SiC gate that is integrated with the anode or the cathode of the isolating diode.

13. The dynamic NVRAM as claimed in claim 5 wherein the isolating diode is a reference-type diode with both forward and reverse *on* operation when the forward and reverse turn-on voltages are exceeded.

14. The dynamic NVRAM of claim 11 wherein the reference diodes are created with either NPN or PNP layers.

15. Dynamic NVRAM in which silicon or silicon-carbide transistors are used as memory elements and silicon-carbide transistors are used as switches connecting the gates of the memory elements.

16. The dynamic NVRAM as claimed in claim 12 in which the gate oxide of the silicon-carbide transistors is prepared by direct oxide growth or by annealing of pre-grown oxide in the presence of NO or N_2O.

17. Volatile Random Access Memory comprising a one-transistor cell with diode isolation of the transistor gates.

18. A metal oxide semiconductor field effect transistor implemented in silicon or silicon carbide with the bit lines crossing the word lines and the sources are in parallel with the word lines.

19. A metal oxide semiconductor field effect transistor as claimed in claim 18 in which the bit lines comprise the MOSFET drains and the word lines comprise the MOSFET gates

20. A MOSFET as claimed in claim 16 in which writing operations are performed with grounded gates.

21. A method of fabricating an NVRAM as claimed in claim 10 or a MOSFET as claimed in claim 16 which includes the step of forming a nitrided silicon oxide gate on the silicon carbide substrate and subsequently carrying out the ion implantation and then finishing the formation of the MOSFET.

22. A method as claimed in claim 18 in which the SiC-SiO_2 interface is passivated by being nitrided at a high temperature in either NO or N_2O environment

23. A method as claimed in claim 19 in which the silicon carbide is a 3C SiC wafer.

24. NVRAM as claimed in claim 12 in which the transistor includes a gate and the gate material is selected from molybdenum, P^+ polysilicon, and platinum silicide.